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Heading : An Ultra-Low Voltage Charge Pump with 83.6% Peak Voltage Conversion Efficiency

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Abstract

The Internet of Things (IOT) facilitates communication between humans and objects, driving the advancement of wearable devices and making them more diverse in terms of functionality and style. Portable sensing devices may experience battery depletion due to prolonged usage, leading to interruptions in monitoring functions. Therefore, an energy harvesting system is necessary to sustain sensor operation. Since the available energy in environment is extremely weak, a power conversion system is required to boost ultra-low voltage to operational voltage range. As a result, a DC-DC boost converter with high conversion efficiency and extremely low operating voltage is crucial. The DC-DC boost convertor could not appropriate controlled while the input is extremely low. A start-up circuit with an ultra-low operating voltage charge pump is important. This paper presents an ultra-low voltage charge pump with 83.6% peak voltage conversion efficiency. The efficiency of proposed circuit is independent while the stages of charge pump increased when input voltage is as low as 100mV. The design was implemented by using 180-nm CMOS process.

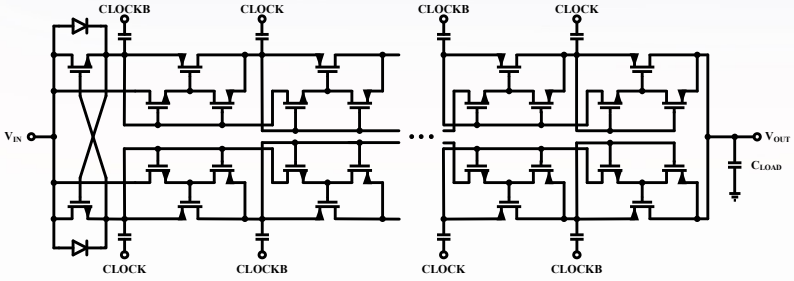
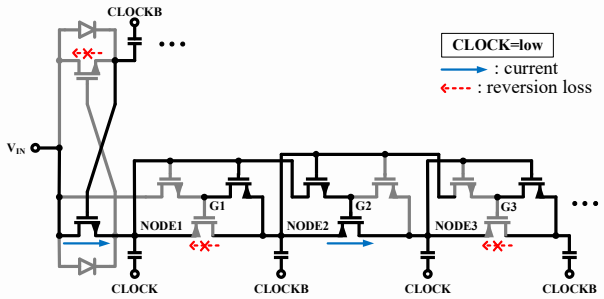


Fig. 1 The Proposed Charge Pump.



(a)

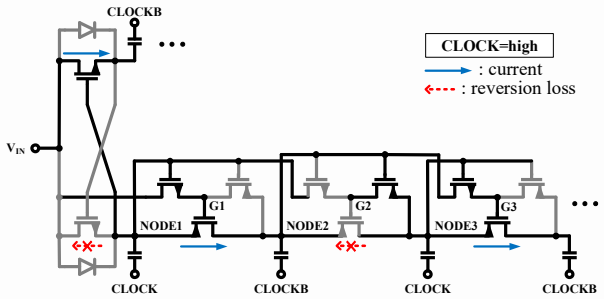
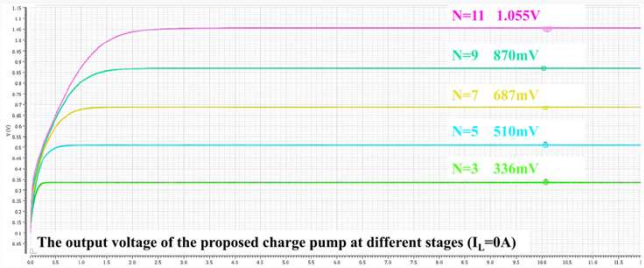
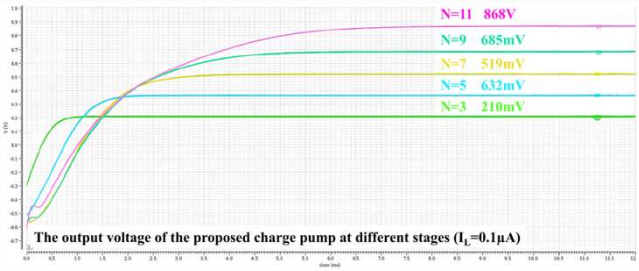


Fig. 2 The proposed charge pump control timing diagram (a) CLOCK is low and (b) CLOCK is high.



(a)



(b)

Fig. 3 The output voltage of proposed charge pump at different stages (a) I_L=0A (b) I_L=0.1μA.

In Fig. 2(b) when CLOCK is high, it is easier to control first stage CTS to turn on. Control signal G1 is connected to the signals of previous two stages, so current flows from NODE1 to NODE2. At the same time, NODE1 turns on PCTS on the other side and turns off PCTS on the same side, avoiding reversion loss from NODE1 back to V_{IN}. Control signal G2 controls second stage CTS to off, preventing reverse loss from NODE3 to NODE2. Simultaneously, the reversion loss of NODE2 flowing to NODE1 and PCTS flowing to V_{IN} on the other side is avoided.

Parameters	TCAS'II 2017	JSSC 2015	MWSCAS 2012	This work
N of Stages	10	3	7	11
Process(nm)	65	130	130	180
Key Technique	Gate-Boosted CCCP	Adaptive Dead-Time CCCP	LCP	LCP with Gate Biasing
Min. Input Vol.(mV)	100	180	125	100
Output Vol. (V) @ I_L=0.1μA	0.76	N/A	0.61	0.868
Peak VCE (%)	76	85.97	58	83.6

Table I Performance summary and comparison

Acknowledgement

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