Tamkang University, ECE, AMOS Lab.
National Kaohsiung Normal University, EE, MSIC Lab.

# Heading: A Multi-Loop Control Adaptive Clocking Digital Low Dropout Regulator with Median Activation Parallel Successive-Approximation Register and Compensation Detect Mechanism

Authors: Wei-Bin Yang, Horng-Yuan Shih, Yu-Lung Lo, Cheng-Ru Yu, Cheng-Kai Lin, Yu-Cheng Chen

## Abstract

**The sensors used in medical devices, such as temperature sensors, humidity sensors, fingerprint sensors, and others, are striving for low power consumption and high performance, driven by the rise of green energy technology. Therefore, in recent years, many system circuits designed for low operating voltage have been proposed, including transceivers, phase-locked loops, oscillators, analog-to-digital converters, and more. To address the aforementioned power requirements, this paper introduces a power management system titled "A Multi-Loop Control Adaptive Clocking Digital Low Dropout Regulator with Median Activation Parallel Successive-Approximation Register and Compensation Detect Mechanism." This system aims to deliver a stable 0.5V voltage output without the need for additional capacitors. Specifically, our contributions include the development of search logic for the entire register control system and the utilization of an adaptive clocking system to generate a 40MHz clock for chasing-state, achieving a settling time of 0.133μs. Furthermore, we reduce the steady-state operating frequency to 1MHz to attain a quiescent current of 12.57μA. Additionally, the compensation loop detection circuit achieves rapid transient response, ensuring that the variation in output voltage remains about 15%. The proposed Low Dropout Regulator is simulated and implemented using the standard 90nm CMOS simulation process.**

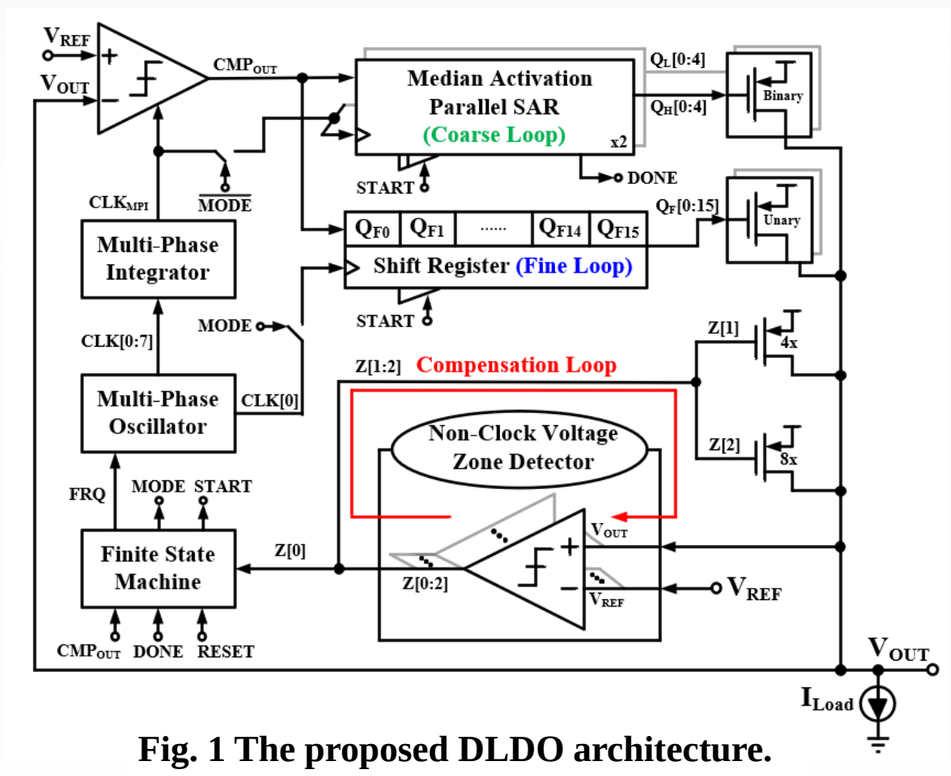


Fig. 1 The proposed DLDO architecture.

Fig.1 introduces a multi-loop control architecture, which divided into three loops: a coarse loop with a larger size, a fine loop with a smaller size, and a compensation loop specifically designed for transient response. This architecture incorporates a voltage zone detector, which converts an external reference voltage, $V_{REF}$, into three sets of internal reference voltages: $V_H$, $V_L$, and $V_{L1}$. It also divides the output voltage into three zones to generate Z[0:2] signals. Fig.2(b) illustrates the operation of the voltage zone detector, and the operational logic is as follows: The Z[0] signal indicates whether the output voltage falls within the VH and VL range. If it does, Z[0] is set to a low state, closing the compensation loop. If not, Z[0] is set to a high state, and the compensation Power MOS for Z[1] or Z[2] are activated based on the extent of voltage undershoot. Therefore, this system can quickly pull back the undershoot voltage for voltage regulation with a response time of less than 5ns to compensate for the transient response.

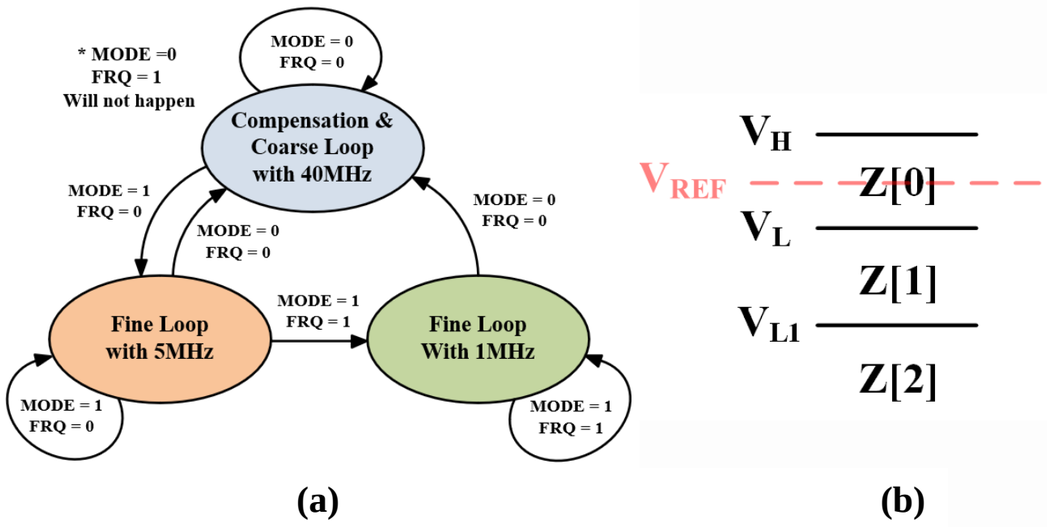


Fig. 2 (a) Adaptive clocking generation logic
(b) The non-clock voltage zone diagram

As shown in Fig.2(a). The clock speed is divided into three states and is controlled by the finite state machine. A clock speed of 40MHz is used to drive the compensation and coarse loops for rapid locking. When the output voltage approaches the target voltage, the MODE signal is triggered, and the fine loop locks at a speed of 5MHz. When the output voltage repeatedly crosses the target voltage, the FRQ signal is triggered, maintaining voltage regulation at a speed of 1MHz. Furthermore, when a transient response occurs, both the MODE and FRQ signals are reset to prepare for the next regulating.

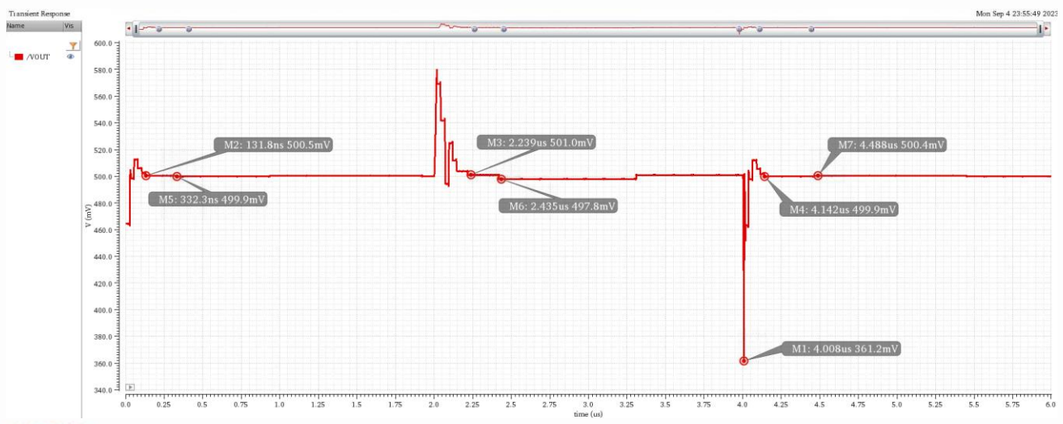


Fig. 3 The proposed DLDO experiment results

| | This Work | TCAS II 2020 | TPE2022 | JSSC2019 | TPE 2021 |
|---|---|---|---|---|---|
| Process | **90nm** | 65nm | 65nm | 65nm | 110nm |
| $V_{IN}$ [V] | **0.6** | 0.6-1.0 | 0.9-1.2 | 0.6-1.2 | 0.8 |
| $V_{OUT}$ [V] | **0.5** | 0.55-0.95 | 0.5-1.1 | 0.4-1.1 | 0.7 |
| $I_{LOAD.MAX}$[mA] | **2.5** | 4.5 | 6 | 100 | 50 |
| $I_Q$[μA] | **12.57** | 10.2 | 131 | 100-1070 | 188.8 |
| $\Delta V_{OUT}$[mV] @$\Delta I_{LOAD}$[mA] | **138.8@2** | 118@4.4 | 80@3 | 108@50 | 360@47.5 |
| $T_{EDGE}$[ns] | **20** | N/A | 5 | 800 | 1 |
| $T_{SET}$[μs] | **0.1327** | 5.9 | 0.09 | 1.24 | 67 |
| $C_{OUT}$[pF] | **1.17** | 1000 | 200 | 40 | 40 |
| $FOM_1$[fF] | **2.04** | 497.36 | 1397.33 | 21.60 | 81.77 |
| $FOM_2$[ns] | **0.57** | 62.17 | 233.00 | 0.9728 | 1.21 |

Table. 1 Performance summary and comparison

$$FOM_1=\frac{C_{OUT}*I_Q*\Delta V_{OUT}}{\Delta I_{LOAD}*V_{OUT}},\ FOM2=I_Q\left(\frac{C_{OUT}*\Delta V_{OUT}}{\Delta I_{LOAD}{}^2}+\frac{0.5}{SR}\right),\ SR=\frac{\Delta I_{LOAD}}{T_{EDGE}}$$